

Control Signals

| Instruction | op[5,4,3,2,1,0] | fc[5,4,3,2,1,0] | RegDst | Branch | MemRd | MemWr | M2R | AluSrc | RegWr | Jump |
|-------------|-----------------|-----------------|--------|--------|-------|-------|-----|--------|-------|------|
| add | 000000 | 100000 | 00 | 0 | 0 | 0 | 000 | 0 | 1 | 00 |
| sub | 000000 | 100010 | 00 | 0 | 0 | 0 | 000 | 0 | 1 | 00 |
| and | 000000 | 100100 | 00 | 0 | 0 | 0 | 000 | 0 | 1 | 00 |
| or | 000000 | 100101 | 00 | 0 | 0 | 0 | 000 | 0 | 1 | 00 |
| nor | 000000 | 100111 | 00 | 0 | 0 | 0 | 000 | 0 | 1 | 00 |
| xor | 000000 | 100110 | 00 | 0 | 0 | 0 | 000 | 0 | 1 | 00 |
| slt | 000000 | 101010 | 00 | 0 | 0 | 0 | 001 | 0 | 1 | 00 |
| addi | 001000 | ----- | 01 | 0 | 0 | 0 | 000 | 1 | 1 | 00 |
| andi | 001100 | ----- | 01 | 0 | 0 | 0 | 000 | 1 | 1 | 00 |
| ori | 001101 | ----- | 01 | 0 | 0 | 0 | 000 | 1 | 1 | 00 |
| xori | 001110 | ----- | 01 | 0 | 0 | 0 | 000 | 1 | 1 | 00 |
| sll | 000000 | 000000 | 00 | 0 | 0 | 0 | 000 | 0 | 1 | 00 |
| srl | 000000 | 000010 | 00 | 0 | 0 | 0 | 000 | 0 | 1 | 00 |
| beq | 000100 | ----- | xx | 1 | 0 | 0 | xxx | 0 | 0 | 00 |
| j | 000010 | ----- | xx | 0 | 0 | 0 | xxx | x | 0 | 01 |
| jr | 000000 | 001000 | xx | 0 | 0 | 0 | xxx | x | 0 | 10 |
| jal | 000011 | ----- | 10 | 0 | 0 | 0 | xxx | x | 0 | 01 |
| lw | 100011 | ----- | 01 | 0 | 1 | 0 | 001 | 1 | 1 | 00 |
| sw | 101011 | ----- | xx | 0 | 0 | 1 | xxx | 1 | 0 | 00 |
| mul | 000000 | 011000 | xx | 0 | 0 | 0 | xxx | 0 | 0 | 00 |
| div | 000000 | 011010 | xx | 0 | 0 | 0 | xxx | 0 | 0 | 00 |
| mfo | 000000 | 010010 | 00 | 0 | 0 | 0 | 011 | 0 | 1 | 00 |
| mfhi | 000000 | 010000 | 00 | 0 | 0 | 0 | 100 | 0 | 1 | 00 |
| lui | 001111 | ----- | 01 | 0 | 0 | 0 | 101 | x | 1 | 00 |

Registers

| | |
|-----------|-------|
| \$zero | 0 |
| \$at | 1 |
| \$v0-\$v1 | 2-3 |
| \$a0-\$a3 | 4-7 |
| \$t0-\$t7 | 8-15 |
| \$s0-\$s7 | 16-23 |
| \$t8-\$t9 | 24-25 |
| \$k0-\$k1 | 26-27 |
| \$gp | 28 |
| \$sp | 29 |
| \$fp | 30 |
| \$ra | 31 |

Instruction Format

